For the sake of discussion, 2 nH is selected to observe the effects of parasitic inductance. The previous circuit description is modified as shown in Fig. 19.14. A new node is created, PARA, that is used to place the inductor between the output node and the capacitor.

Running the simulation with the added parasitic inductor yields a transfer function that has similar characteristics up to a decade past f_C, and then a notch is observed, after which the attenuation actually decreases because of the inductor's increasing impedance at high frequencies (Fig. 19.15). Increasing the parasitic inductance, as would be experienced with a leaded capacitor, would cause the notch to move to lower frequencies in simulation.

Transmission line analysis can be performed with Spice's transient analysis capability. Different termination circuits and transmission line topologies can be investigated in varying degrees of detail, depending on the accuracy of the models used. It may be difficult to generate an accurate model of an IC driver or receiver, but relatively good estimates can be obtained by combining multiple ideal elements. The circuit shown in Fig. 19.16 uses a pulse voltage source with a 5-Ω series resistor to simulate the driver's output resistance and an inductor to represent the IC package's lead inductance.

```
V1          VIN 0 DC 0Vdc AC 1Vac
R1          VIN VOUT 75
L1          PARA VOUT 2nh
C1          0 PARA 220p
.AC DEC 10 1e5 1e9
.PROBE
.END
```

FIGURE 19.14 Bode magnitude plot for RC filter with parasitic inductance.

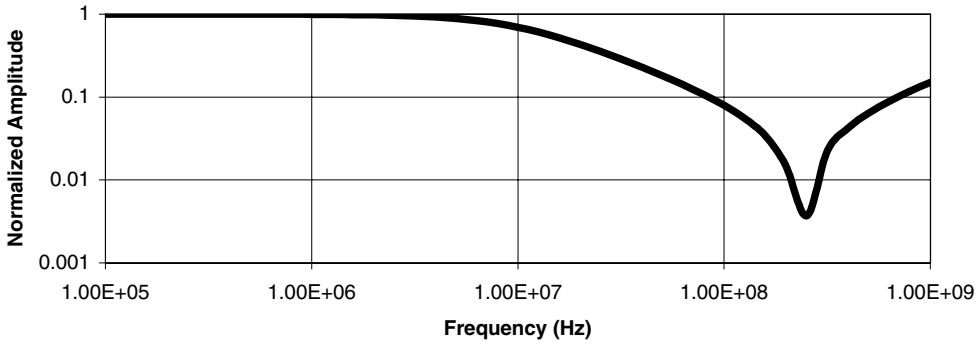

FIGURE 19.15 Bode magnitude plot for RC filter with parasitic inductance.

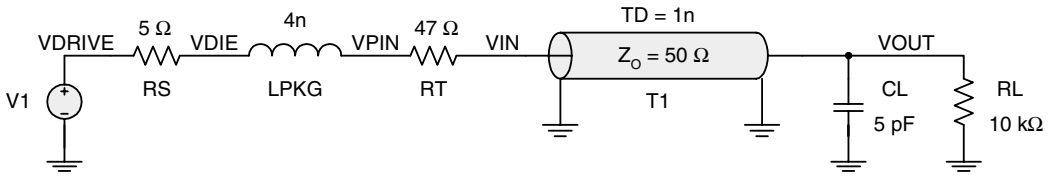

FIGURE 19.16 Transmission line circuit.

A 47-Ω series termination resistor connects the simulated driver to a 50-Ω transmission line model that has a delay of 1 ns, corresponding to a physical length of approximately 6 in (15 cm). The load is represented by a 10-kΩ resistance to ground and 5 pF of shunt capacitance.

Each node in the circuit is uniquely named so that the circuit can be represented in Spice's description format. Spice supports a variety of voltage and current sources. Voltage sources can emit constant DC levels; sine waves of varying phase, frequency, and amplitude; pulses; and other forms of circuit stimulation. The pulse voltage source is chosen for this transmission line analysis with a period of 10 ns, rise and fall times of 1 ns, and a 50 percent duty cycle to simulate a 100-MHz clock driver. Figure 19.17 shows the circuit description for the circuit in Fig. 19.16. Note the `+PULSE` specification following the voltage source declaration that specifies amplitude when off, amplitude when on (3.3-V driver is simulated), delay, rise time, fall time, high time, and period. The delay can be used to shift the pulse and is set here arbitrarily to 1 ns. Ideal lossless transmission lines are represented with a T prefix and are specified with ground nodes at the input and output as well as characteristic impedance and delay.

Following the circuit description is the `.TRAN` command that instructs Spice to perform a transient analysis for 120 ns and to display the results only after 100 ns. The first 100 ns are used to establish steady-state conditions so that the results are not affected by the circuit state at time zero when all elements are discharged. Waiting for a circuit to stabilize is not necessary in all cases and could have been omitted here with little effect. The first parameter to `.TRAN` is the step size, which is set to 0 to use the best simulation resolution. Selecting a larger step size shortens the simulation, which may be desirable for certain long analyses.

Figure 19.18 shows the plotted simulation results from the transmission line analysis showing minimal distortion. Little overshoot and undershoot are observed. How well this simulation matches a real laboratory observation depends on the accuracy of the circuit model and the accuracy of the observation. An ideal transmission line model is used in this example. If a good quality PCB with ground plane is used and stub lengths on termination components are minimized, the results should match relatively well. If the driver has significantly different output impedance, there will be less of a correlation.

One of the benefits of using Spice is the ability to try many different test cases to gain an understanding of how variance in certain circuit parameters affects the circuit's behavior. If a parameter is varied slightly, and the behavior changes dramatically, a warning should be recognized that the circuit is sensitive and small differences between the model and reality can cause trouble. Variation in driver output impedance, termination resistance, and transmission line impedance are useful parameters for experimentation. Fig. 19.19 shows the simulation results of the transmission line circuit with a 33-Ω termination resistor instead of a 47-Ω device. This simulation is done not to experiment with variance of purchased resistors but to examine the effects of a significantly different termina-

```
V1          VDRIVE 0
+PULSE 0 3.3 1n 1n 1n 4n 10n
RS          VDRIVE VDIE  5
RT          VPIN VIN  47
LPKG        VDIE VPIN  4n
T1          VIN 0 VOUT 0 Z0=50 TD=1ns
CL          0 VOUT  5p
RL          0 VOUT  10k
.TRAN  0 120ns 100n
.PROBE
.END
```

FIGURE 19.17 Spice circuit description for transmission line analysis.